Features

- **Programmable Interval Timer**
- **Three Independent 16-bit Counters**
- **Optional Single-byte and BCD Modes**
- **Status Read-back Command**
- **Full Register and Standard Software Compatibility**
- **Low Power Consumption for Battery-powered Applications**
- **Approximately 3450 Gates**

Description

The CB_8254 Macrocell is a programmable interval timer with a control register and three independent 16-bit timer/counters that can be programmed over a common 8-bit CPU interface. It can be used for timing external events, producing fixed delays or producing repetitive waveforms.

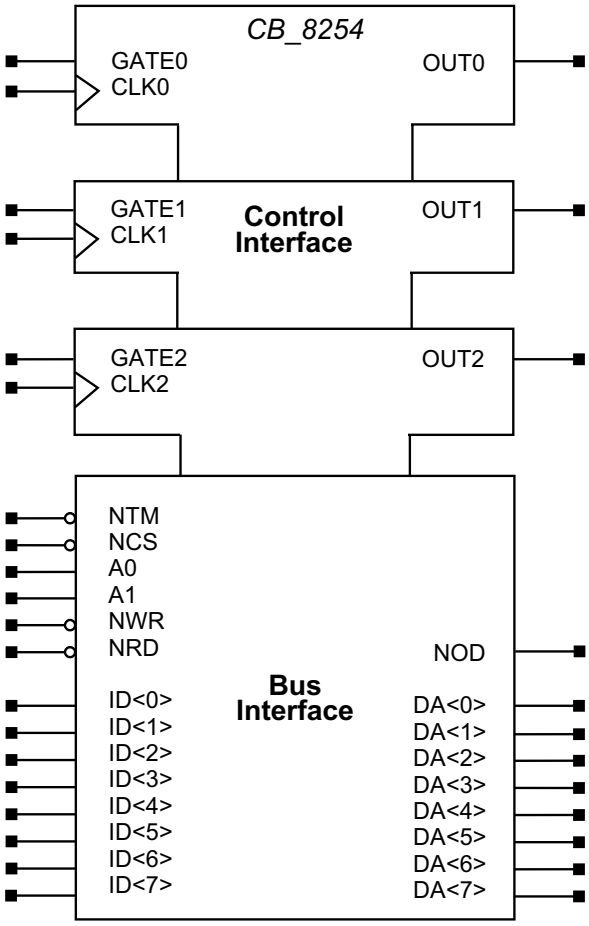
The design forms part of the Atmel Macrocell Library which includes other Macrocell functions required for PC, XT and PC/AT motherboard Asic designs. The CB_8254 is compatible with the industry standard 8254 device.

Standard Interface Macrocell

CB_8254 Programmable Interval Timer

0885A/cb_8254.fm5–8/97

Pin Description



The function of the I/O signals is the same as the original 8254, except that the bi-directional data bus is split into an 8-bit input bus and an 8-bit output bus.

Table 1. Control Interface

Signal Name	Type	Description
GATE0	Input	Gate input to counter 0
CLK0	Input	Clock input to counter 0
OUT0	Output	Zero count output from counter 0
GATE1	Input	Gate input to counter 1
CLK1	Input	Clock input to counter 1
OUT1	Output	Zero count output from counter 1
GATE2	Input	Gate input to counter 2
CLK2	Input	Clock input to counter 2
OUT2	Output	Zero count output from counter 2

Table 2. Bus Interface

Signal Name	Type	Description
NTM	Input	Test mode - active low
NCS	Input	Device Chip select - active low
A0, A1	Input	Address lines to device
NWR	Input	Write Strobe - active low
NRD	Input	Read Strobe - active low
ID 0-7	Input	Input Data bus
NOD	Output	Not Data output
DA 0-7	Output	Output Data bus

Operating Modes

There are six modes of operation for the counters. The mode is defined by the contents of the mode bits of the control register. In all modes the counters operate as down counters. They are defined as follows:

Mode 0: Interrupt on Terminal Count

Mode 1: Hardware Retriggerable One-Shot

Mode 2: Rate Generator

Mode 3: Square Wave Mode

Mode 4: Software Triggered Strobe

Mode 5: Hardware Triggered Strobe (Retriggerable)

Test Modes

There are 10 test strobes, which are used in test mode to decrement the higher nibbles of the three counters, and to do a special test mode form of reset. Test mode is entered by taking the test pin low. The strobes take effect when the data lines or the address lines are toggled.

Table 3. Test Strobes

Signal Name	Test Strobe Definition
ID0	Counter0, Nibble 1
ID1	Counter0, Nibble 2
ID2	Counter0, Nibble 3
ID3	Counter1, Nibble 1
ID4	Counter1, Nibble 2
ID5	Counter1, Nibble 3
ID6	Counter2, Nibble 1
ID7	Counter2, Nibble 2
A0	Counter2, Nibble 3
A1	Test mode special reset