Features

- **Industry-standard USART (Universal Synchronous/Asynchronous Receiver Transmitter)**
- **Synchronous and Asynchronous Operation**
- **Full Duplex Operation**
- **Support for most Serial Data Formats including IBM bi-sync Operation**
- **Supports Clock Inputs of 1X, 16X and 64X the required Baud Rates in Asynchronous Modes**
- **Full Register and Standard Software Compatibility**
- **Low power Consumption for Battery-powered Applications**
- **Gate Count: Approximately 2100 Gates**

Description

The CB_8251A macrocell can transmit and receive in both synchronous and asynchronous modes. In each of the four cases, a standard protocol is followed. There is a HUNT mode for synchronization with an incoming data stream. Checks are carried out for parity, framing and overrun errors.

The device has two modes of operation - synchronous mode and asynchronous mode. The mode of operation is determined by a software write to the mode register. Programming the CB_8251A requires accessing registers at the same address in a sequence, where the register addressed is determined by the point in the sequence. There is a recovery time of 6 CLK cycles between each write to the command channel.

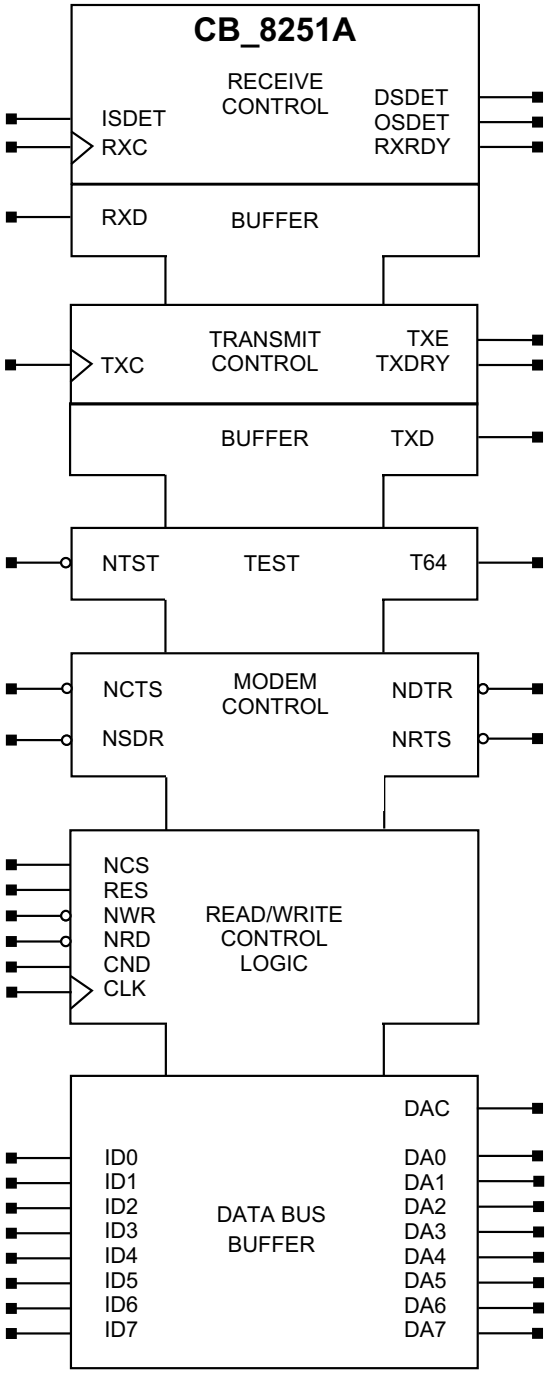
The CB_8251A macrocell is designed to be compatible with the industry standard 8251A USART (Universal Synchronous / Asynchronous Receiver Transmitter). The CB_8251A Macrocell follows the same pinout, with the exception of bi-directional pins which are split into input and output pins with a direction control pin for use with bi-directional buffers and the addition of two pins which are used in test mode. Some signal names have also been modified in order to avoid problems with CAD systems.

Standard Interface Macrocell

CB_8251A USART

0883A/cb_8251a.fm5–09/97

Pin Description



The pinout of the CB_8251A follows that of the original device, except that bi-directional pins are split into input and output pins. As a result there are 18 output pins and 21 input pins used by the macro, all of these are used by the test vectors supplied.

Table 1. Receiver Signals

Signal Name	Type	Description
ISDET	Input	With external sync mode selected, a high level commands the CB_8251A to start receiving characters on the next RXC rising edge.
RXC	Input	Receive clock, either 1x, 16x or 64x the asynchronous baud rate, or 1x the synchronous baud rate
DSDET	Output	Direction control for bi-direct version of STET pin. High is input, Low is output.
OSDET	Output	High true. In asynchronous mode, goes high when a break condition is detected. In synchronous mode, goes high when SYNC is detected and internal sync mode is selected.
RXRDY	Output	High true, indicating that the receive buffer has data for the CPU
RXD	Input	Receive data.

Table 2. Transmission Signals

Signal Name	Type	Description
TXC	Input	Transmit clock, either 1x, 16x or 64x the asynchronous baud rate, or 1x the synchronous baud rate
TXE	Output	High true, indicating TX buffer is empty
TXRDY	Output	High true, indicating that the TX buffer is ready to accept data
TXD	Output	Transmit data

Table 3. Test Pins

Signal Name	Type	Description
NTST	Input	When low test modes can be accessed
T64	Output	Clock divide output

Table 4. Modem Control

Signal Name	Type	Description
NCTS	Input	Clear to send - low enables a transmission, if Tx is enabled
NDSR	Input	Data set ready
NDTR	Output	Data terminal ready
NRTS	Output	Request to send

Table 5. CPU Bus Signals

Signal Name	Type	Description
NCS	Input	CPU chip select strobe (active low)
RES	Input	When high for more than 6 CLK cycles, the CB_8251A is forced into its idle state.
NWR	Input	CPU data write strobe (active low)

Test Mode

There are five test modes which are entered by taking the NTST pin to a logic 0. These are defined as follows:

- NTSO: NTST= 0, ID1 = 1: Test data input to second stage of SYNC detection circuit. End of RX state machine sequence.
- NST3: NTST= 0, ID3 = 1: Fast step TX state machine.
- NTS4: NTST= 0, ID4 = 1: Fast step RX state machine.
- NTS5: NTST= 0, ID5 = 1: Write to Mode word out of sequence.
- NTWR: NTST= 0, NWR= 0: a software reset.

Table 5. CPU Bus Signals

Signal Name	Type	Description
NRD	Input	CPU data read strobe (active low)
CND	Input	When high selects Command channel, when low selects Data channel
CLK	Input	A clock with a frequency of greater than 30 times RXC and TXC in synchronous mode and X1 asynchronous mode, and 4.5 times RXC and TXC in X16 and X64 asynchronous mode.
DAC	Output	Bi-directional data bus control line. When low data is output, when high data is input.
ID7-ID0	Input	CPU data input
DA7-DA0	Output	CPU data output